WHAT IS CLAIMED IS:

1. An apparatus comprising:

a first microvia pad;

a second microvia pad having a projection extending in a direction toward the first microvia pad; and

a microvia electrically coupled to the first microvia pad and to the second microvia pad.

2. An apparatus according to Claim 1, wherein the microvia includes a plurality of surfaces facing a plurality of surfaces of the projection.

3. An apparatus according to Claim 1, wherein the projection is an integral portion of the second microvia pad.

4. An apparatus according to Claim 1, further comprising:

an electroless conductor disposed between the microvia and the second microvia pad,

wherein the second microvia pad and the microvia are composed of an electrolytic conductor.

5. An apparatus according to Claim 1, further comprising:

an integrated circuit package including a plurality of metallization layers,

wherein a first one of the metallization layers includes the first microvia pad, and a second one of the metallization layers includes the second microvia pad.

6. An apparatus comprising:

a first microvia pad;

a second microvia pad; and

a microvia electrically coupled to the first microvia pad and to the second microvia pad, the microvia including a plurality of surfaces facing respective ones of a plurality of surfaces of the second microvia pad.

7. An apparatus according to Claim 6, further comprising:

an electroless conductor disposed between the microvia and the second microvia pad,

wherein the second microvia pad and the microvia are composed of an electrolytic conductor.

8. An apparatus according to Claim 6, further comprising:

an integrated circuit package including a plurality of metallization layers,

wherein a first one of the metallization layers includes the first microvia pad, and a second one of the metallization layers includes the second microvia pad.

9. A method comprising:

fabricating a microvia pad having a base and a projection extending from the base; and

fabricating a microvia having a plurality of surfaces facing a plurality of surfaces of the projection.

10. A method according to Claim 9, further comprising:

fabricating an electroless conductor disposed between the microvia and the microvia pad,

wherein the microvia pad and the microvia are composed of an electrolytic conductor.

11. A method according to Claim 10, wherein fabricating the microvia pad comprises:

fabricating the base; and

fabricating the projection extending from the base after fabricating the base.

12. A system comprising:

an integrated circuit package comprising:

a first microvia pad;

a second microvia pad having a projection extending in a direction toward the first microvia pad; and

a microvia electrically coupled to the first microvia pad and to the second microvia pad; and

a double data rate memory electrically coupled to the integrated circuit package.

13. A system according to Claim 12, wherein the microvia includes a plurality of surfaces facing a plurality of surfaces of the projection.

14. A system according to Claim 12, wherein the projection is an integral portion of the second microvia pad.

15. A system according to Claim 12, further comprising:

a motherboard electrically coupled to the integrated circuit package and to the memory.

16. An apparatus comprising:

an integrated circuit package core; and

a microvia having a first portion adjacent to a first microvia pad and a second portion adjacent to a second microvia pad, a width of the first portion being greater than a width of the second portion,

wherein a distance between the first portion and the integrated circuit package core is less than a distance between the second portion and the integrated circuit package core.

17. An apparatus according to Claim 16, further comprising:

a second microvia having a third portion adjacent to a third microvia pad and a fourth portion adjacent to a fourth microvia pad, a width of the third portion being greater than a width of the fourth portion,

wherein a distance between the third portion and the integrated circuit package core is less than a distance between the fourth portion and the integrated circuit package core.

18. An apparatus according to Claim 17,

wherein the first microvia is adjacent to a first side of the integrated circuit package core, and the second microvia is adjacent to a second side of the integrated circuit package core.

19. An apparatus according to Claim 16, further comprising:

a plurality of metallization layers,

wherein a first one of the metallization layers includes the first microvia pad, and a second one of the metallization layers includes the second microvia pad.

20. A method comprising:

fabricating a signal routing device on a substrate, the signal routing device comprising a microvia having a first portion and a second portion, a width of the first portion being greater than a width of the second portion;

removing the signal routing device from the substrate; and

attaching the signal routing device to an integrated circuit package core, wherein a distance between the first portion of the microvia and the integrated circuit package core is less than a distance between the second portion of the microvia and the integrated circuit package core.

21. A method according to Claim 20, wherein the signal routing device is attached to a first side of the integrated circuit package core, the method further comprising:

fabricating a second signal routing device on a second substrate, the second signal routing device comprising a second microvia having a third portion and a fourth portion, a width of the third portion being greater than a width of the fourth portion;

removing the second signal routing device from the second substrate; and

attaching the second signal routing device to a second side of the integrated circuit package core, wherein a distance between the third portion of the microvia and the integrated circuit package core is less than a distance between the fourth portion of the microvia and the integrated circuit package core.

22. A method according to Claim 20, wherein the signal routing device is attached to a first side of the integrated circuit package core, the method further comprising:

fabricating a second signal routing device on the substrate, the second signal routing device comprising a second microvia having a third portion and a fourth portion, a width of the third portion being greater than a width of the fourth portion;

removing the second signal routing device from the substrate; and

attaching the second signal routing device to a second side of the integrated circuit package core, wherein a distance between the third portion of the microvia and the integrated circuit package core is less than a distance between the fourth portion of the microvia and the integrated circuit package core.

23. A method according to Claim 20, wherein fabricating the signal routing device on the substrate comprises fabricating the signal routing device on a release layer attached to the substrate.

24. A system comprising:

an integrated circuit package comprising:

an integrated circuit package core; and

a microvia having a first portion adjacent to a first microvia pad and a second portion adjacent to a second microvia pad, a width of the first portion being greater than a width of the second portion,

wherein a distance between the first portion and the integrated circuit package core is less than a distance between the second portion and the integrated circuit package core; and

a double data rate memory electrically coupled to the integrated circuit package.

25. A system according to Claim 24, the integrated circuit package further comprising:

a second microvia having a third portion adjacent to a third microvia pad and a fourth portion adjacent to a fourth microvia pad, a width of the third portion being greater than a width of the fourth portion,

wherein a distance between the third portion and the integrated circuit package core is less than a distance between the fourth portion and the integrated circuit package core.

26. A system according to Claim 25, wherein the first microvia is adjacent to a first side of the integrated circuit package core, and the second microvia is adjacent to a second side of the integrated circuit package core.

27. A system according to Claim 24, further comprising:

a motherboard electrically coupled to the integrated circuit package and to the memory.